CLAIMS

What is claimed is:

1. A method comprising:

accessing a plurality of data read requests received from an input/output (I/O) interface and stored in a first order;

generating a plurality of read entries from the plurality of data read requests, the plurality of read entries identifying a plurality of data reads to read data to service the plurality of data read request;

storing the plurality of read entries in the first order;

selecting a different second order to submit the plurality of data reads.

2. The method of claim 1, further comprising:

servicing a data read of a first read entry;

then servicing a data read of a second read entry prior to completing servicing the data read request corresponding to the first read entry.

3. The method of claim 2, wherein servicing includes:

submitting the plurality of data reads to a memory according to the different second order; and

receiving return data in accordance the data read requests.

4. The method of claim 2, further comprising:

storing the plurality of data read requests in the first order according to the order the data read requests are received in over time; and

removing a completed data read request from the first order after completion of servicing of the completed data read request, wherein the completed data read request is the first received data read request.

5. The method of claim 1, wherein selecting includes:

identifying each data read as a pop, a fetch, or a prefetch;

determining whether at least one data read identified as a fetch is eligible to issue as a fetch;

identifying a next data read to service from the plurality of data reads as an eligible data read identified as a fetch, if a data read identified as a fetch is eligible to issue as a fetch;

determining whether at least one data read identified as a prefetch is eligible to issue as a prefetch, if at least one data read identified as a fetch is not eligible;

identifying a next data read to service from the plurality of data reads as an eligible data read identified as a prefetch, if at least one data read identified as a prefetch is eligible to issue as a prefetch.

6. The method of claim 5, wherein a pop removes a data read request from the first order after completion of servicing of the data read request, a fetch returns data from a main memory or a cache memory to a data read requester, and a prefetch returns data from main memory to a cache memory.

7. The method of claim 5, wherein determining whether at least one data read identified as a fetch is eligible includes reviewing a selected fetch read entry of the at least one data read identified as a fetch a selected number of times until either a data read identified as a fetch and eligible to issue as a fetch is found, or until each of the at least one data read identified as a fetch for the fetch selected read entry is reviewed at least once; and determining whether a data read identified as a prefetch is eligible includes reviewing a selected prefetch read entry of the at least one data reads identified as prefetches the selected number of times until either a data read identified as a prefetch and eligible to issue as a prefetch is found, or until each of the at least one data reads identified as prefetch for the selected prefetch read entry is reviewed at least once.

8. The method of claim 5, further comprising:

submitting the next data read to a central arbiter to read data from a first memory;

receiving return data identified by the data read request; and

one of writing the return data to a second memory and returning the return data to a requester of a data read request that the next data read satisfies.

9. The method of claim 7, wherein submitting the next data read includes obtaining from the stored data read request a memory address, a requester identification, a tag, and a byte enable flag.

10. The method of claim 1, wherein the plurality of data read request are received from one of a device that supports one of an input/output (I/O) specification and a peripheral components interconnect express (PCI-E) specification.

11. The method of claim 1, wherein the plurality of read entries correspond to a subset of the plurality of data read requests.

12. The method of claim 1, wherein each data read is to read at least one cache line sized read of data defined by a central arbiter and the data read request is to request a total number of cache lines requested by a data read requester.

13. The method of claim 1, wherein each read entry includes information identifying: (1) whether the read entry has valid data, (2) a total number of cache lines requested by a data read request, and (3) an identification of a portion of the total number of cache lines already serviced by data fetches.

14. An apparatus comprising:

a storage structure to store a plurality of read entries in a first order, the plurality of read entries derived from a plurality of data read requests to be received from an input/output (I/O) interface and to be stored in the first order, the plurality of read entries to identify a plurality of data reads to service the plurality of data read request;

a controller coupled to the storage structure to submit the plurality of data reads in a different second order.

15. The apparatus of claim 14, wherein the different second order is submitted to read data from a plurality of memories.

16. The apparatus of claim 14, further comprising a control arbiter to service a data read of a first read entry, then servicing a data read of a second read

entry prior to completing servicing the data read request corresponding to the first read entry.

17. The apparatus of claim 14, further comprising logic to implement an arbitration scheme to select a next data read to service from the plurality of data reads.

18. The apparatus of claim 14, further comprising logic to derive each read entry from a corresponding data read request, wherein each read entry includes at least one data read and the at least one data read is sufficient to complete servicing of the corresponding data read request.

19. A system comprising:

a FIFO to store a plurality of data read requests in a in a first order, the data read requests to be received from an input/output (I/O) interface;

a storage structure to store a plurality of read entries in the first order, each read entry derived from a data read request;

a controller coupled to the storage structure to submit to a central arbiter to read data from a memory a plurality of data reads from the read entries to service a data read of a first read entry, and then servicing a data read of a second read entry prior to completing servicing the data read request corresponding to the first read entry.

20. The system of claim 19, wherein the FIFO includes compact register file memory and the storage structure includes standard memory cell logic.

21. The system of claim 19, wherein the plurality of data reads are to be submitted to a digital communication chip.

22. The system of claim 19, wherein the controller includes control logic to implement an arbitration scheme to service the read entries in a different second order from an main memory and an cache memory.